In The Claims:

Claim 1. (currently amended) An electrostatic discharge (ESD) device used with a high-voltage input pad, wherein the ESD device is disposed between the high-voltage input pad and an internal circuit, ~~serving as a secondary device in a two-stage protection circuit, and~~ comprising:

~~a substrate;~~

a primary device disposed on a substrate, wherein the primary device is coupled to the high-voltage input pad and the internal circuit; and

a secondary device disposed on the substrate between the primary device and the internal circuit, wherein the secondary device comprising:

a first MOS transistor ~~disposed on the substrate,~~ comprising a first gate, a first drain and a first source, wherein the first gate is coupled to a bias Vg1, and the first drain is coupled to the high-voltage input pad; and

a second MOS transistor ~~disposed on the substrate,~~ comprising a second gate, a second drain and a second source, wherein the second gate and the second source are both grounded, and the second drain is electrically connected with the first source of the first MOS transistor.

Claim 2. (original) The ESD device of claim 1, wherein each of the first MOS transistor and the second MOS transistor comprises a NMOS transistor.

Claim 3. (original) The ESD device of claim 1, wherein the first MOS transistor comprises a non-LDD NMOS transistor.

Claim 4. (original) The ESD device of claim 1, wherein an input voltage from the high-voltage input pad is higher than 10V.

Claim 5. (original) The ESD device of claim 1, wherein Vg1 is 3.3V.

Claim 6. (original) The ESD device of claim 1, wherein the substrate comprises a P-type substrate.

Claim 7. (currently amended) A programmable memory apparatus, comprising:

a substrate;

a programmable memory device on the substrate;

a high-voltage input pad on the substrate electrically connected with the memory device; and

a two-stage protection circuit disposed on the substrate and coupled between the memory device and the high-voltage input pad, the two-stage protection circuit comprising a primary device and a secondary device, wherein the secondary device is disposed between the primary device and the programmable memory device, and the secondary device comprises:

a first MOS transistor disposed on the substrate, comprising a first gate, a first drain and a first source, wherein the first gate is coupled to a bias Vg1, and the first drain is coupled to the high-voltage input pad; and

a second MOS transistor disposed on the substrate, comprising a second gate, a second drain and a second source, wherein the second gate and the second source are both grounded, and the second drain is electrically connected with the first source of the first MOS transistor.

Claim 8. (original) The programmable memory apparatus of claim 7, wherein each of the first MOS transistor and the second MOS transistor comprises a NMOS transistor.

Claim 9. (original) The programmable memory apparatus of claim 7, wherein the first MOS transistor comprises a non-LDD NMOS transistor.

Claim 10. (original) The programmable memory apparatus of claim 7, further comprises a resistor coupled between the primary device and the secondary device.

Claim 11. (original) The programmable memory apparatus of claim 7, wherein an input voltage from the high-voltage input pad is higher than 10V.

Claim 12. (original) The programmable memory apparatus of claim 7, wherein Vg1 is 3.3V.

Claim 13. (original) The programmable memory apparatus of claim 7, wherein the substrate comprises a P-type substrate.